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(54) Integrated circuit chip having an identification circuit therein

(57) A semiconductor integrated circuit chip (1) comprises a chip identification circuit (20) which includes a voltage limiter (22) for limiting the input potential difference between a power voltage supply terminal (Vss or VDD) and an input terminal (IN1), and an option means (24) connected to said voltage limiter (22) for determining the identification information of the chip according to whether or not a current path is formed (24) during manufacture of the chip. A chip identification test is carried out through the existing input and output terminals and power supply terminals without the need for extra test and diagnostic pins and without the aid of laser equipment or the like.

FIG. 1

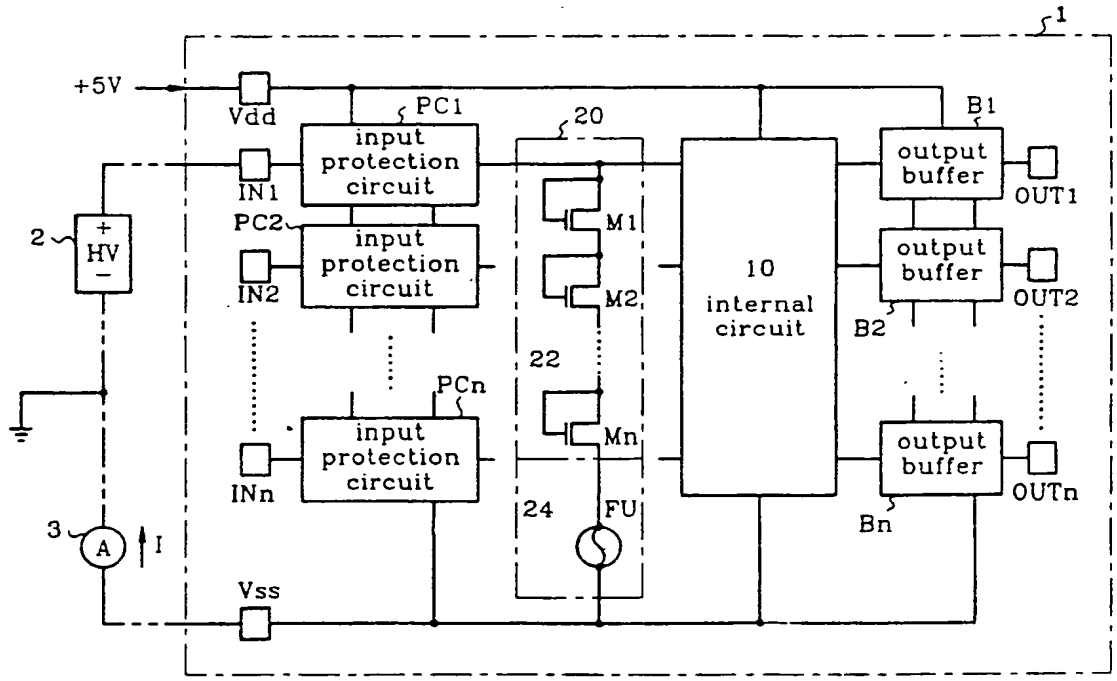

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FIG. 1

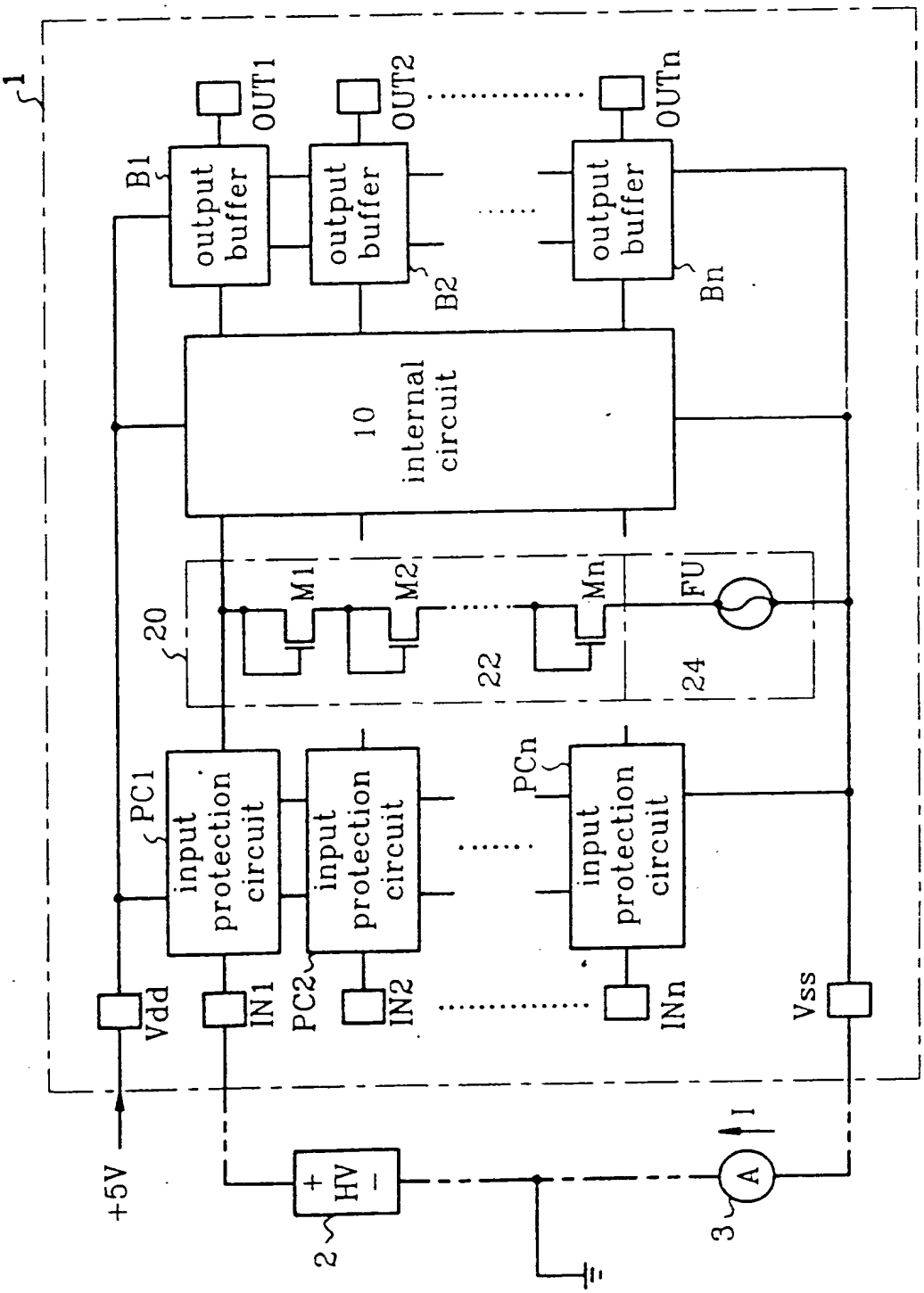

1
OUT1
OUT2
OUTn
B1
B2
Bn
output buffer
output buffer
output buffer
10
internal circuit
20
M1
M2
Mn
FU
22
24
PC1
PC2
PCn
input protection circuit
input protection circuit
input protection circuit
Vdd
IN1
IN2
INn
Vss
+5V
HV
2
A
I
3

FIG.2

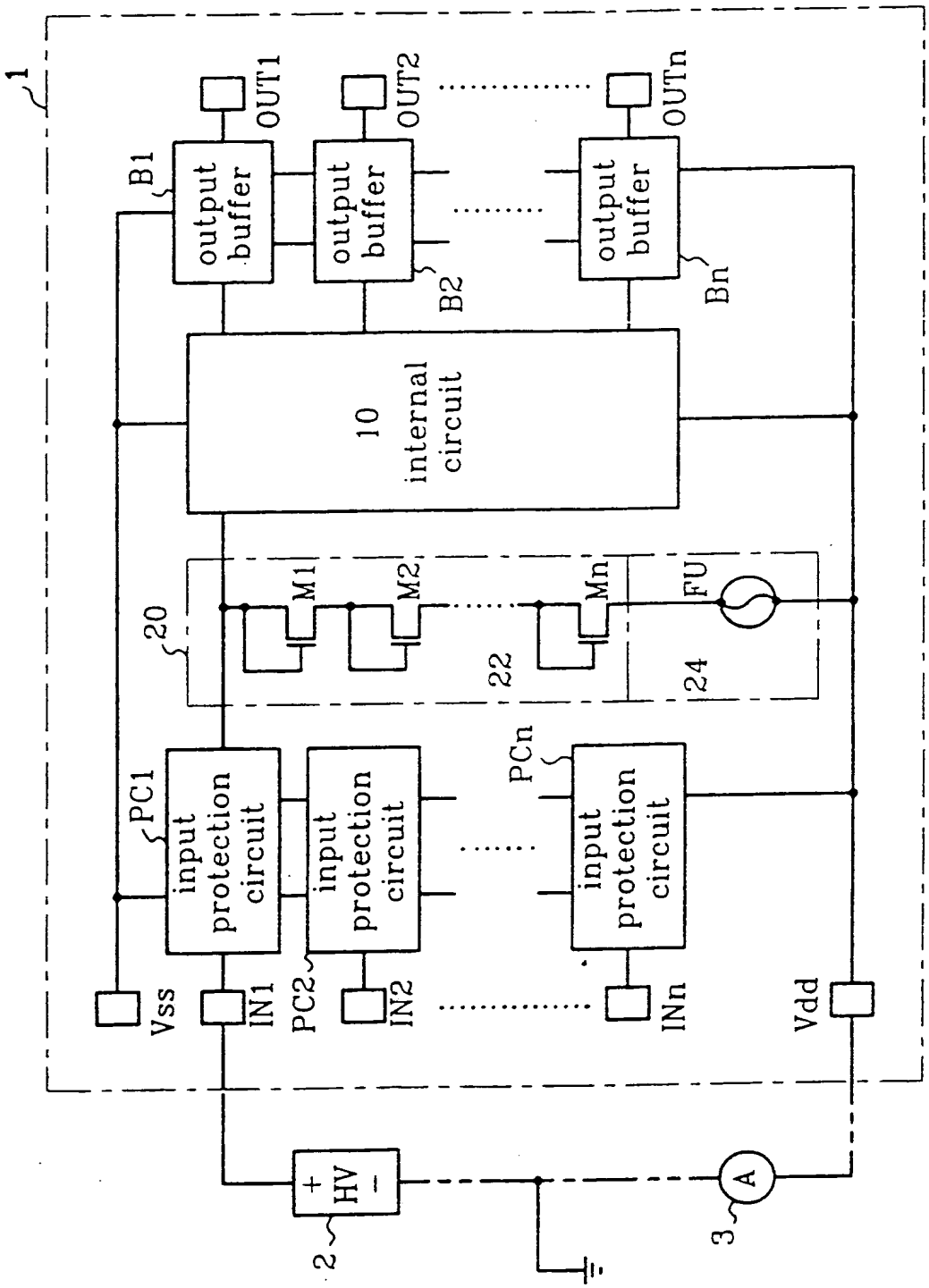

1
OUT1
OUT2
OUTn
B1
B2
Bn
output buffer
output buffer
output buffer
10
internal circuit
20
M1
M2
Mn
FU
22
24
PC1
PC2
PCn
input protection circuit
input protection circuit
input protection circuit
Vss
IN1
IN2
INn
Vdd
+
HV
−
2
A
3

FIG.3

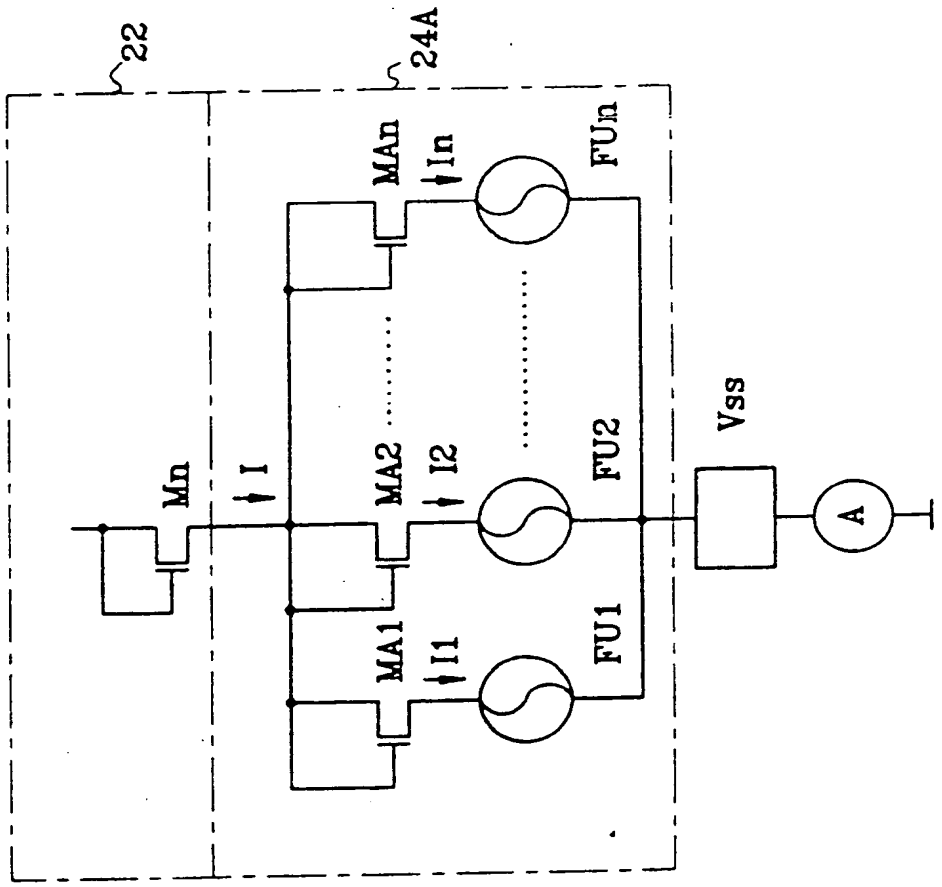
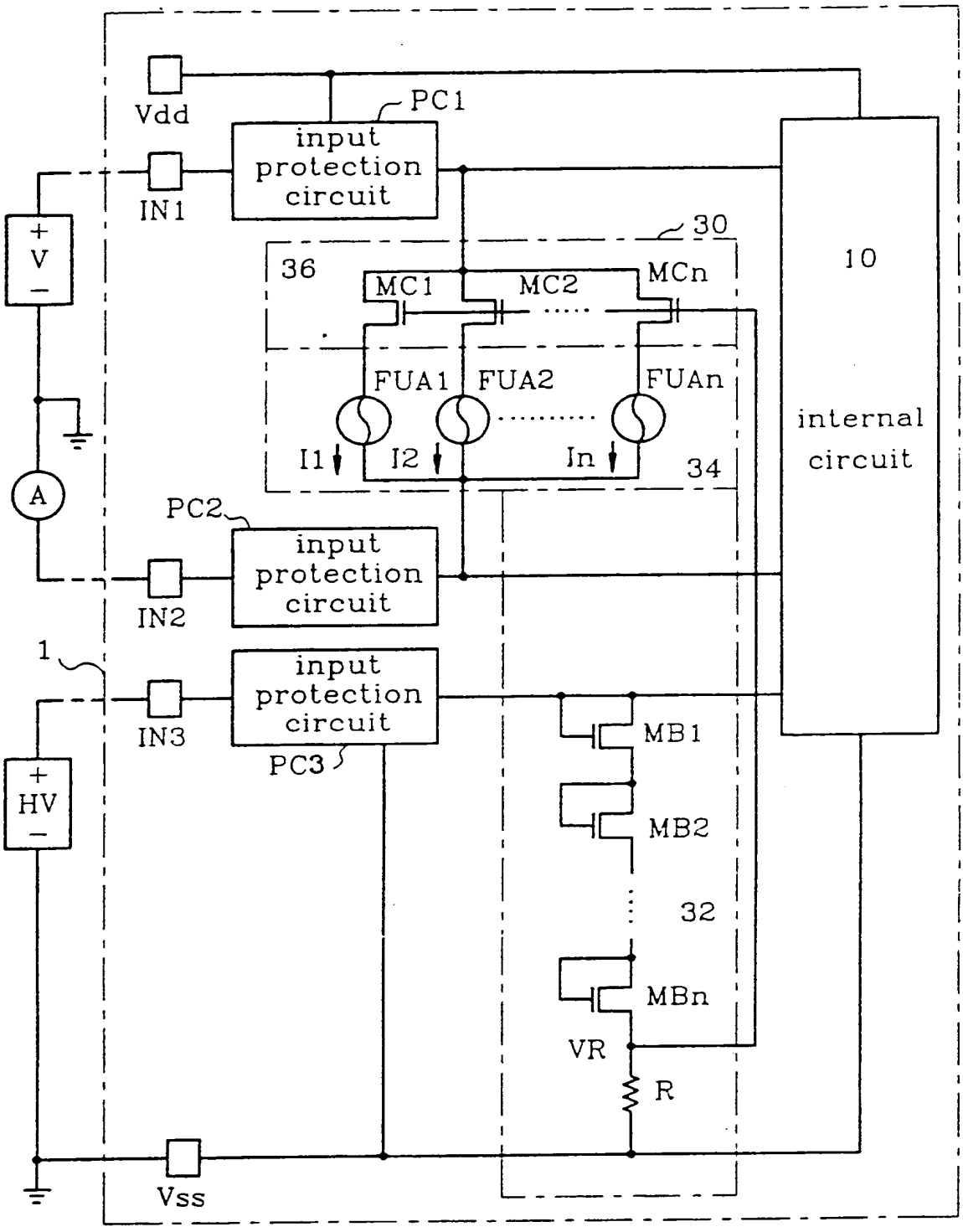


FIG.4


Vdd
PC1
input protection circuit
IN1
+ V −
30
36
MC1
MC2
MCn
10
FUA1
FUA2
FUAn
internal circuit
I1
I2
In
34
A
PC2
input protection circuit
IN2
1
input protection circuit
IN3
PC3
MB1
MB2
32
MBn
VR
R
+ HV −
Vss

SEMICONDUCTOR INTEGRATED CIRCUIT CHIP HAVING AN IDENTIFICATION CIRCUIT THEREIN

The present invention relates to a semiconductor integrated circuit chip, more particularly, to a semiconductor integrated circuit (IC) chip having an identification circuit within the chip for sorting chips by means of a test.

Recently, there has been a growing tendency for electronic systematisation to be accomplished over the whole field of industry in accordance with the development of semiconductor techniques. Consequently, the suitable characterization of electronic systems is required to meet the peculiarity of each field. For that reason, semiconductor manufacturers have sought diversification of products to satisfy the various demands of the users. For example, various operating modes, in addition to a basic operating mode, have been developed as the storage capacity of the DRAM has been increased to M bit. That is, in 1M or 4M DRAM, the operating modes are divided into 1bit, 4bit, 8bit etc., according to the number of an output data and are divided into a fast page mode, a nibble mode, a static column mode etc., according to an input control signal. Therefore, in order to satisfy the user's demands, DRAM suppliers are providing various DRAMs performing the different modes according to various selected modes, by optionally providing the specific operating modes besides a basic operating mode of the DRAM during the manufacturing process thereof. For example, the fast page mode is taken as the basic operating mode in a single DRAM manufacturing line and the nibble or the static column mode DRAM

is produced by optionally providing the operating mode during the manufacturing steps, respectively.

Such an optional provision is performed wafer by wafer and the manufactured DRAMs are divided into each mode. Subsequently, after a DRAM has been manufactured, during an assembling process, the wafer is separated into an individual die or chip through a scribing process, the separated dies are packaged into a specific package through the processes of a die mounting, a wire bonding and a molding, and the packaged DRAM will be forwarded as a final product after marking the data of the product, e.g., the serial number, manufacture date and manufacturing line through the test of the product.

However, in case of a DRAM manufactured by the aforesaid process, the dies or chips divided into each mode often become mixed up with other kinds of chips when producing the dies or chips in a single line. In this case, the products of the different operation modes are checked as erroneous chips during the next test step and are treated as an article of inferior quality, resulting in yield reduction.

Also, to prevent one kind of die from being mixed with other kinds of dies, very careful attention is required, thereby reducing operation efficiency.

Accordingly, a technique is required that makes it possible to sort or to identify the chip types during the test step, when chips having different modes are mixed with one another before packaging.

Such an identifying technique of the semiconductor chips has been disclosed in U.S. patent Nos. 4,150,331 and 4,510,673.

In the U.S. patent No. 4,150,331, a technique is disclosed that identifies each chip by using a programmable circuit device on the chip surface. The circuit device is to program an identification code according to whether a diode is formed or not between an additionally provided test and diagnostic pin and selected input/output pin.

However, the aforementioned technique has a defect in that the package size, which has an important effect on the price of semiconductor chip, becomes larger because the extra test pin is provided.

In U.S. patent No. 4,510,673 a technique is disclosed with which the specific identification mark is indicated on the back surface of semiconductor chip by using a laser apparatus. This identification mark can be distinguished by human or machine by using laser or optical apparatus. However, this technique has a defect in that expensive laser apparatus is required to provide the specific identification mark, e.g., a manufacturing line, manufacture date. An object of present invention is to provide a semiconductor integrated circuit chip having a new identification circuit that does not need an extra test and diagnostic pin and solves the above mentioned problems in the prior art.

An object of an embodiment of the present invention is to provide a semiconductor integrated circuit chip having an identification circuit that is simple in construction and facilitates the identification of the semiconductor chip.

According to one aspect of the present invention, there is provided a semiconductor integrated circuit chip having a pair

of power voltage supply terminals and a plurality of input terminals and an identification circuit means connected between any one of the power voltage supply terminals and any one of the input terminals, wherein

said identification circuit means comprises:

a voltage limiter having a predetermined limiting voltage level for limiting the input potential difference between said one of the power voltage supply terminals and said one of the input terminals; and

an option means connected in series with said voltage limiter for determining the identification information of said chip according to whether or not a current path is formed during the manufacturing process of said chip. According to a further aspect of the present invention, there is provided a semiconductor integrated circuit chip having a pair of power voltage supply terminals and at least three input terminals and an identification circuit means connected with any one of said power voltage supply terminals and connected with three of said at least three input terminals, wherein

said identification circuit means comprises:

a voltage limiter having a predetermined limiting voltage level for limiting the input potential difference between said one of said power voltage supply terminals and one of said three input terminals and then generating a predetermined control voltage by dividing the limited voltage level; an option means connected between the remaining two of said three input terminals for determining the identification information of said chip according to whether or not a current path is formed during the

manufacturing process of said chip; and

a switch means connected in series with said option means, said switch means being turned on by said control voltage supplied from said voltage limiter.

With these configuration, the present invention can adopt an identification circuit for a chip without adding an extra pin such as test and diagnostic pin.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

FIG. 1 is a simplified representation of an embodiment of a semiconductor integrated circuit chip having an identification circuit according to the present invention;

FIG. 2 is a simplified representation of another embodiment of a semiconductor integrated circuit chip having an identification circuit according to the present invention;

FIG. 3 is a circuit diagram showing a modification of an option means shown in FIG. 1 and FIG. 2, and

FIG. 4 illustrates in simplified form still another embodiment of a semiconductor integrated circuit chip having an identification circuit according to the present invention.

FIG. 1 depicts in schematic form an embodiment of a semiconductor integrated circuit chip having an identification circuit according to the present invention. In FIG. 1, an integrated circuit chip 1 includes an internal circuit 10, input protection circuits PC1 to PCn, output buffers B1 to Bn, input terminals IN1 to INn, output terminals OUT1 to OUTn and a pair of power supply terminals Vdd and Vss. The IC chip is connected

to a power source, not shown herein, so as to receive power voltage of, for instance, 5V via the power voltage supply terminal Vdd and receives a ground potential via the power voltage supply terminal Vss. The internal circuit 10 receiving the operating voltage from said power voltage supply terminals Vdd and Vss, performs a given function by receiving input signals supplied at the input terminals IN1 to IN3 and generates predetermined output signals through the output terminals OUT1 to OUTn. Also, said input terminals IN1 to INn are connected to the internal circuit 10 via the respective input protection circuits PC1 to PCn which prevent the breakage of internal circuit 10 due to a noise voltage, for example, surge or the like, supplied to the input terminals.

The output terminals OUT1 to OUTn are connected with the internal circuit 10 via output buffers B1 to Bn, respectively.

An identification circuit 20, the characterising feature of the present invention, is connected between one terminal IN1 of the input terminals and the power voltage supply terminal Vss of the IC chip 1. This identification circuit comprises a voltage limiter 22 and an option means 24. The voltage limiter 22 is provided for level-limiting an input signal supplied between the input terminal IN1 and the power voltage terminal Vss to a predetermined logic level which is to be supplied to the internal circuit 10. This voltage limiter 22 consists of a plurality of serially connected MOS transistors M_1 to Mn of which the respective gates are connected to the respective drains thereof. Also, the voltage limiter 22 can set the predetermined logic level by the sum of threshold voltages of each MOS transistor.

For example, the predetermined logic level will be set to approximately more than 2.5V when TTL level is supplied to the input terminal; and approximately more than +3V when CMOS level is supplied to the input terminal.

Although, the diode-configuration of MOS transistor, is used in this embodiment, it will be noted that any unilateral current flow device having a predetermined threshold voltage, for example, PN junction diode or Zener diode or the like, may be used as the voltage limiter.

The option means 24 is provided for determining a current flow passing through the voltage limiter 22 during the manufacturing process and is connected to the voltage limiter 22 in series. To provide the option means 24, a simple option processing technique is used wherein connection or disconnection of a fuse or metal wire formed during the manufacturing process determines the mode of the chip. In this embodiment, after the fuse has been formed, the identification information of chips are written by the option process wherein melting off of the fuse through laser zappling process is determined.

For example, during the manufacturing process of the chip, the fuse FU in a chip is kept connected for a DRAM of fast page mode operation; and is melted off for a DRAM of nibble mode operation, thereby making possible the chip identification. During a test step of the chip fabrication process for the aforementioned identification processed chip, the input terminal IN1 is connected to a predetermined high voltage source 2, for example, a voltage source of an approximately 15V and the power voltage supply terminal Vss is connected to an ammeter 3, by

which it is possible to distinguish the mode of the DRAM. If the current flows, the sample is identified as a DRAM for high page mode operation, whereas if the current does not flow, it is identified as DRAM of nibble mode operation, by means of the ammeter 3.

Here, in case of nibble mode, the fuse is melted off so that the input signal is transferred to the internal circuit 10 regardless of the existence of the identification circuit 20 during the normal operation of the chip; but in the case of high page mode, if it were not for the voltage limiter 22, the input terminal IN1 would always be in the state of logic 0 through the fuse Fu. The occurrence of this phenomenon will be prevented by the voltage limiter 22. In more detail, when logic "0" is applied to the input terminal IN1, logic "0" is inputted to the internal circuit 10 regardless of the connection of the identification circuit 20; but when logic "1" is applied to the input terminal IN1, the current flows through the identification circuit 20, thus generating a predetermined voltage difference in the voltage limiter 22 which causes the internal circuit 10 to be inputted with logic "1".

The identification circuit 20 is preferably connected to the input terminal IN1 through the input protection circuit PC1 which protects the identification circuit from damage due to external surge or the like.

FIG. 2 illustrates another embodiment of the semiconductor integrated circuit chip according to the present invention, wherein the circuit configuration is the same as that of the previous embodiment except that the identification circuit 20 is

connected between the power voltage supply terminal Vdd and the input terminal IN1. Since the voltage of +15V supplied to the input terminal is higher than the voltage of +5V supplied from the power voltage supply terminal Vdd during the identification test, the underlying principles of operation of the chip is the same as that of the previous embodiment.

FIG. 3 illustrates a modification of the option means 24 for identifying two or more kinds of chips. As shown in FIG. 3, the option means 24 comprises a plurality of MOS transistors MA1 to MAn the gates of which are connected to the drains thereof and a plurality of fuses FU1 to FUn respectively connected to the respective MOS transistors. Each combination of a MOS transistor and a fuse is connected in parallel one another between the voltage limiter 22 and the power voltage supply terminal Vss (Vdd).

In order to identify the chips by the circuit as constructed above, identification information may be given by the current values passing through the option means as shown in Table 1.

Table 1

	fuse connection			identification information
	FU 1	FU 2	FU 3	
fast page mode	connected	connected	connected	$I_1+I_2+I_3$
nibble mode	melted	connected	connected	I_2+I_3
static column mode	melted	melted	connected	I_3
other mode	melted	melted	melted	0

FIG. 4 shows a modification of the identification circuit for identifying two or more kinds of chips. In FIG. 4, the identification means 30 is connected with the power source supply terminal Vss and three input terminals IN1 to IN3. The identification means 30 comprises a voltage limiter 32, an option means 34 and a switch means 36.

The voltage limiter 32 is constructed such that it should limit the input voltage difference applied between the input terminal IN3 and power supply terminal Vss to the logic level received in the internal circuit 10 then divide the given logic level to generate a predetermined control voltage VR. The voltage limiter 32 comprises a plurality of MOS transistors MB1 to MBn whose gates are connected to the drains thereof and a resistor R connected to the MOS transistors, said plurality of MOS transistors and the resistor being connected between the input terminal IN3 and the power supply terminal Vss. The voltage distributed between the two terminals of the resistor R is supplied to the switch means 36 as a control voltage VR. The switch means 36 is serially connected to the option means between the input terminals IN1 and IN2 to switch the current flow to be turned on by the control voltage VR of said voltage limiter 32. The switch means 36 consists of a plurality of MOS transistors MC1 to MCn wherein the drain of each transistor is connected to the input terminal IN1; the gates are applied with the control voltage VR; and the sources are connected to the corresponding fuses of the option means 34 described later.

In this embodiment, the option means 34 consists of a plurality of fuses FUA1 to FUAn each of which is connected

to the corresponding MOS transistor of said switch means 36. Each combination of a MOS transistor and a fuse is connected in parallel with one another between the input terminals IN1 and IN2. Here, the melting of the respective fuses of the option means are carried out during the manufacturing process of the chip to provide the required identification information.

In order to identify the chips provided with the identification circuit of the above described embodiment, the input terminal IN1 is connected with a power source V of a predetermined voltage of, for example, 5V, the input terminal IN2 is connected with an ammeter A and a power source of higher voltage of, for example, 15V is connected between the input terminal IN3 and the power supply terminal Vss. Upon supply of these power sources, current flows through voltage limiter 32 and a predetermined voltage is distributed in the resistor R, generating the control voltage VR to be supplied to the switch means 36. Due to the control voltage VR, the respective MOS transistors MC1 and MCn of the switch means 36 becomes turned on. Thus, the current flow between the input terminals IN1 and IN2 is indicated on the ammeter A. Here, the current values are obtained as shown in the Table 2 according to which, if any, of fuses FUA1 to FUAn are melted off.

Table 2

fuse connection state			identification information
FUA1	FUA2	FUA3	
connected	connected	connected	$I_1+I_2+I_3$
melted	connected	connected	I_2+I_3
melted	melted	connected	I_3
melted	melted	melted	0

It is noted that in Table 2 the chips can be written with the identification information which can identify four different chip modes.

When the chip is not in the chip identification test, the ground voltage is supplied to the gates of the respective MOS transistors MC1 to MCn of the switch means 36 via the resistor VR, thus ensuring the normal operation of the chip.

As described above, according to the present invention, the chip identification information is written through the optional provision of the connection or disconnection of such simple circuit during the wafer manufacturing process. The written identification information is detected in the test step of the usual assembly process of the chip so that chips of the same kind can be detected and treated separately in the subsequent process.

With the chip of the present invention, the chip identification test is carried out through existing input and output terminals and power supply terminals differently from the conventional method, so that the conventional manufacturing system is utilized to the utmost without requiring any change

thereof, which is very economical and desirable.

Further, the chip of the present invention does not require an extra test and diagnosis pin and expensive laser equipment or the like for identifying the chip.

It should be noted that the chip according to the present invention has been described as being useful for the MOS transistors in the above embodiments, but can be adapted to various applications upon request. Thus, the present chip can be modified in various forms within the scope of the present invention.

CLAIMS

1. A semiconductor integrated circuit chip having a pair of power voltage supply terminals and a plurality of input terminals and an identification circuit means connected between any one of said power voltage supply terminals and any one of said input terminals, wherein said identification circuit means comprises:

a voltage limiter having a predetermined limiting voltage level for limiting the input potential difference between said one of said power voltage supply terminals and said one of said input terminals; and

an option means connected in series with said voltage limiter for determining the identification information of the chip according to whether or not a current path is formed during the manufacturing process of the chip.

2. A semiconductor integrated chip as defined in claim 1, wherein said voltage limiter comprises a plurality of serially connected MOS transistors whose respective gates are connected to the drains thereof, whereby said predetermined limiting voltage level is set to be the sum of the threshold voltages of said MOS transistors.

3. A semiconductor integrated circuit chip as defined in claim 1 or 2, wherein said option means consists of a fuse connection or disconnection of which is obtained during the manufacturing process of the chip.

4. A semiconductor integrated circuit chip as defined in any preceding claim, wherein said option means consists of a metal wire disposed between the gate and the source of a MOS transistor connected to said voltage limiter, said metal wire

being formed during a metalization step of the manufacturing process of said chip.

5. A semiconductor integrated circuit as defined in any of claims 1 to 3, wherein said option means comprises a plurality of combinations of a MOS transistor whose gate is connected to the drain thereof and a fuse connected to the source of said MOS transistor, said combinations being connected in parallel with each other and the identification information of said chip being set according to the number of said fuses which are melted off.

6. A semiconductor integrated circuit chip having a pair of power voltage supply terminals and at least three input terminals and an identification circuit means connected with any one of said power voltage supply terminals and connected with three of said at least three input terminals, wherein said identification circuit means comprises:

a voltage limiter having a predetermined limiting voltage level for limiting the potential difference between said one of said power voltage supply terminals and one of said three input terminals and then generating a predetermined control voltage by dividing the limited voltage level; an option means connected between the remaining two of said three input terminals for determining the identification information of said chip according to whether or not a current path is formed during the manufacturing process of said chip; and

a switch means connected in series with said option means, said switch means being turned on by said control voltage supplied from said voltage limiter.

7. A semiconductor integrated circuit chip as defined in

claim 6, wherein said voltage limiter comprises:

a plurality of serially connected MOS transistors whose respective gates are connected to the respective drains thereof; and

a resistor connected to said plurality of MOS transistors, said limited voltage level being the sum of the terminal voltage of said resistor and the threshold voltages of said MOS transistors and said control voltage being said terminal voltage of said resistor.

8. A semiconductor integrated circuit chip as defined in claim 6 or 7, wherein said option means comprises a plurality of fuses and said switch means comprises a plurality of MOS transistors, each of said plurality of fuses being serially connected to a respective one of said plurality of MOS transistors, said MOS transistors being turned on by said control voltage applied to gates thereof, and said identification information of said chip being determined according to the number of said fuses melted off.

9. A semiconductor integrated circuit chip having an identification circuit therein, substantially as hereinbefore described with reference to Figures 1 to 4 of the accompanying drawings.

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